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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,244	01/23/2002	Katsuhito Sasaki	OKI.295	5830

7590 10/01/2003  
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EXAMINER	
GARCIA, JOANNIE A	
ART UNIT	PAPER NUMBER

2823  
DATE MAILED: 10/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/052,244	SASAKI, KATSUHITO
Examiner	Art Unit	
Joannie A Garcia	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

**A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.**

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on \_\_\_\_.
- 2a) This action is **FINAL**.      2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.
- 4) Claim(s) **1-18** is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_ is/are allowed.
- 6) Claim(s) **1-18** is/are rejected.
- 7) Claim(s) \_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Disposition of Claims**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on **23 January 2002** is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on \_\_\_\_ is: a) approved b) disapproved by the Examiner.  
 If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
 \* See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
 a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_.
- 4) Interview Summary (PTO-413) Paper No(s). \_\_\_\_.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: \_\_\_\_.

The finality of the Office Action mailed 04-07-03 has been withdrawn in view of applicant's argument.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 2, 7-12, and 14, are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "high" in claims 2, 8 and 14, is a relative term, which renders the claims indefinite. The term "high" is not defined by the claims, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. If applicant intends a particular ion implantation energy, it should be clearly recited.

In claim 7, line 5, --region-- should be preceded by "within the first well".

In claim 7, line 12, --region-- should be preceded by "within the second well".

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "104" and "104a" have both been used to designate first insulating film. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 5-8, 11-14, 17, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Efland et al (U.S. Patent 5,736,766).

Efland et al discloses manufacturing an LDMOS transistor 10 comprising providing a semiconductor substrate 11 of a first conductivity type having a well region 38 of a second conductivity type formed on a surface thereof (Figure 2, and Column 3, lines 21-34), implanting ions of the first conductivity type into a part of the well region with an energy (Figure 4, and Column 3, lines 61-63), thermally growing a gate oxide layer 56 on the surface of the semiconductor substrate, diffusing the implanted ions to form a diffusion region 46 of the first conductivity type on the surface of the semiconductor substrate (Figures 5-6, and Column 4, lines 25-28), forming a gate electrode 58 on the surface of the semiconductor substrate (Figure 7, and Column 4, lines 30-40), and forming a reduced surface drain 62 on the surface of the semiconductor substrate within the first region (Figure 8, and Column 4, lines 45-51), wherein the implantation energy could be set so that an accelerated oxidation during a formation of the gate oxide layer is inhibited (Figure 8), and wherein said implantation is conducted into a region of the semiconductor substrate where the drain region is formed (Figures 4 and 8).

Efland et al discloses as well, manufacturing an LDMOS transistor 10 comprising providing a semiconductor substrate 11 of a first conductivity type having a first well 38

of a second conductivity type formed on a surface thereof within a first region (Figure 2, and Column 3, lines 30-33), and a second well 46 of the first conductivity type formed within a second region that is inside of the first region (Figure 5, and Column 3, lines 60-63), implanting ions of the second conductivity type into the second well with an energy (Column 3, lines 26-27), thermally growing a gate oxide layer 56 on the surface of the semiconductor substrate, diffusing the implanted ions to form a diffusion region 48 of the second conductivity type located in a third region that is inside of the second region (Figures 5-6, and Column 4, lines 25-28), forming a gate electrode 58 on the surface of the semiconductor substrate (Figure 7), the gate oxide layer extending from the first region to the third region through the second region (Figure 6), and forming a reduced surface drain 62 on the surface of the semiconductor substrate within the first region (Figure 3, and Column 4, lines 19-20), wherein the implantation energy could be set so that an accelerated oxidation during said formation of the gate oxide layer is inhibited (Figure 8), and wherein said implantation is conducted into a region of the semiconductor substrate where the drain region is formed (Figure 8).

Claims 3, 4, 9, 10, 15 and 16, are rejected under 35 U.S.C. 103(a) as being unpatentable over Efland et al as applied to claims 1, 2, 5-8, 11-14, 17, and 18 above, and further in view of the following comments.

Efland et al does not teach that said implantation is conducted at an energy of about 500 KeV with a dose of about  $5.0 \times 10^{15} / \text{cm}^2$ . It would have been a matter of routine optimization within the teachings of Efland et al to determine a suitable energy and dose to achieve the implantation step of Efland et al.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is (703) 308-0956. See **MPEP 203.08.**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner J. Garcia whose telephone number is (703) 306-5733. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax number for this group is (703) 308-7722 (and 7724), and (703) 305-3431 (and 3432). MPEP 502.01 contains instructions regarding procedures used in submitting responses by facsimile transmission.

  
JAG  
9/16/03

  
George Fourson  
Primary Examiner